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Analog & Mixed Signal Verification Engineer

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Company: Chipright

Location: United Kingdom

Category: architecture-and-engineering

Senior Analog & Mixed Signal Verification Engineerponsibilities will include:

Perform verification simulations and generate design documentation for ASIC development projects

Design suitable test benches in both Virtuoso Analog Design Environment or VHDL as necessary

Present results to the ASIC project team to feedback block performance

Flag any performance issues early in the design cycle

Generate verification reports and design documents for all key blocks

Lead/participate in peer design reviews

Generate ASIC operation manual

The role may also include definition and design for some sections of the ASIC, predominantly digital functionality with Virtuoso Digital Implementation (VDI) and RTL.

Contribute to any continuous improvement initiatives

Essential Skills and Experience:

A good degree (BEng/MEng) in Electronic/Electrical Engineering

Minimum 3-4 years in relevant industry in a development role

Cadence tool suites : predominantly analog (Virtuoso) but with experience to the digital flow

Ability to extract simulation results, capture in a document and present to the team for peer review

Cadence administration knowledge would be an advantage

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